

**Amendments to the Claims:**

Claims 1-23 have been canceled. New claims 24-31 have been added. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

Claims 1-23. (Canceled)

24. (New) A printed circuit board, comprising:  
a substrate; and  
an electrically conductive layer disposed on at least one side of the substrate, comprising;  
a voltage reference plane substantially covering the at least one side of the substrate and  
configured for operable coupling to a voltage reference signal;  
a plurality of signal trace slots formed in the voltage reference plane; and  
a plurality of signal traces disposed in the plurality of signal trace slots;  
wherein the plurality of signal traces are electrically isolated from the voltage reference  
plane by a gap in the electrically conductive layer with a gap distance sufficient to  
avoid an electrical short between the plurality of signal traces and the voltage  
reference plane; and  
wherein the voltage reference plane forms a continuous electrical connection around each  
of the plurality of signal trace slots such that at least a portion of the voltage  
reference plane is disposed between any two of the plurality of signal traces to  
reduce cross talk between signals carried by the any two of the plurality of signal  
traces.
25. (New) The electronic device of claim 24, further comprising a passivation layer  
disposed on the electrically conductive layer.

26. (New) The printed circuit board of claim 24, wherein at least one of the plurality of signal traces includes at least one direction change in the length thereof over the substrate.

27. (New) The printed circuit board of claim 24, wherein at least a portion of the plurality of conductive traces are embodied as vias.

28. (New) The printed circuit board of claim 24, wherein the substrate includes:  
an electrically insulative layer disposed on the electrically conductive layer; and  
an additional electrically conductive layer disposed on the electrically insulative layer,  
comprising;  
an additional voltage reference plane substantially covering the electrically insulative  
layer and configured for operable coupling to the voltage reference signal;  
a plurality of additional signal trace slots formed in the additional voltage reference plane;  
and  
a plurality of additional signal traces disposed in the plurality of additional signal trace  
slots;  
wherein the plurality of additional signal traces are electrically isolated from the  
additional voltage reference plane by an additional gap in the additional  
electrically conductive layer with an additional gap distance sufficient to  
avoid an electrical short between the plurality of additional signal traces  
and the additional voltage reference plane; and  
wherein the additional voltage reference plane forms a continuous electrical  
connection around each of the plurality of additional signal trace slots such  
that at least a portion of the additional voltage reference plane is disposed  
between any two of the plurality of additional signal traces to reduce cross  
talk between signals carried by the any two of the plurality of additional  
signal traces.

29. (New) The printed circuit board of claim 28, wherein at least a portion of the plurality of signal traces are operably coupled to at least a portion of the plurality of additional signal traces by vias formed through the electrically insulative layer.

30. (New) The printed circuit board of claim 28, wherein the voltage reference plane is operably coupled to the additional voltage reference plane by vias formed through the electrically insulative layer.

31. (New) An electronic system, comprising:  
a processor;  
a memory device;  
at least one input device;  
at least one output device; and  
at least one data storage device;  
wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes a printed circuit board comprising:  
a substrate; and  
an electrically conductive layer disposed on at least one side of the substrate, comprising:  
a voltage reference plane substantially covering the at least one side of the substrate and configured for operable coupling to a voltage reference signal;  
a plurality of signal trace slots formed in the voltage reference plane; and  
a plurality of signal traces disposed in the plurality of signal trace slots;  
wherein the plurality of signal traces are electrically isolated from the voltage reference plane by a gap in the electrically conductive layer with a gap distance sufficient to avoid an electrical short between the plurality of signal traces and the voltage reference plane; and

wherein the voltage reference plane forms a continuous electrical connection around each of the plurality of signal trace slots such that at least a portion of the voltage reference plane is disposed between any two of the plurality of signal traces to reduce cross talk between signals carried by the any two of the plurality of signal traces.